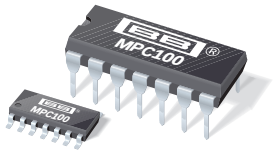
BURR - BROWN®



MPC100

Wide Bandwidth 4 x 1 VIDEO MULTIPLEXER

FEATURES

- BANDWIDTH: 250MHz (1.4Vp-p)
- LOW INTERCHANNEL CROSSTALK: ≤60dB (30MHz, DIP); ≤70dB (30MHz, SO)
- LOW SWITCHING TRANSIENTS: +2.5/–1.2mV
- LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.05%, 0.01°
- LOW QUIESCENT CURRENT: One Channel Selected: ±4.6mA No Channel Selected: ±230µA

APPLICATIONS

- VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)
- RADAR SYSTEMS
- DATA ACQUISITION
- INFORMATION TERMINALS
- SATELLITE OR RADIO LINK IF ROUTING

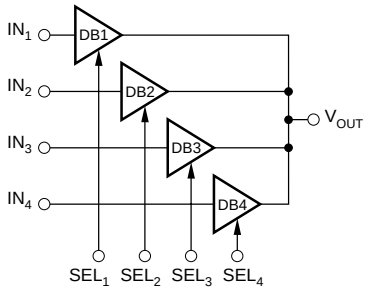
DESCRIPTION

The MPC100 is a very wide bandwidth 4-to-1 channel video signal multiplexer which can be used in a wide variety of applications.

MPC100 is designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC100 make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC100 consists of four identical monolithic integrated open-loop buffer amplifiers, which are connected internally at the output. The unidirectional transmission path consists of bipolar complementary buffers, which offer extremely high output-to-input isolation. The MPC100 multiplexer enables one of the four input channels to connect to the output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL-input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 250MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of 4nV/√Hz make this crosspoint switch suitable for RF and video applications. All performance is specified with ±5V supply voltage, which reduces power consumption in comparison with ±15V designs. The multiplexer is available in space-saving SO-14 and DIP packages. Both are designed and specified for operation over the industrial temperature range (–40°C to +85°C.)



TRUTH TABLE

SEL_1	SEL_2	SEL_3	SEL_4	V_{OUT}
0	0	0	0	HI-Z
1	0	0	0	IN_1
0	1	0	0	IN_2
0	0	1	0	IN_3
0	0	0	1	IN_4

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1133F
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SPECIFICATIONS

At V_{CC} = ±5V, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

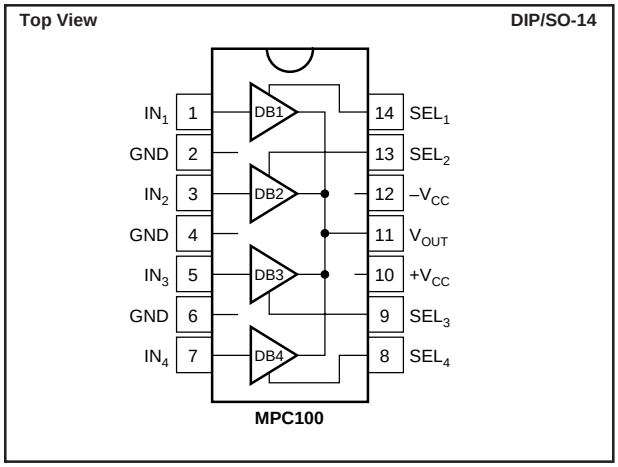
PARAMETER	CONDITIONS	MPC100AP, AU MIN	MPC100AP, AU TYP	MPC100AP, AU MAX	UNITS
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE	R_{IN} = 0, R_{SOURCE} = 0				
Initial			+10	±30	mV
vs Temperature			±30		µV/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V	–40	–80		dB
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		–50		dB
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–50		dB
Initial Matching	Between the Four Channels		±3		mV
INPUT BIAS CURRENT					
Initial			+4	±10	µA
vs Temperature			20		nA/°C
vs Supply (Tracking)	V_{CC} = ±4.5V to ±5.5V		±380		nA/V
vs Supply (Non-tracking)	V_{CC} = +4.5V to +5.5V		+1.0		µA/V
vs Supply (Non-tracking)	V_{CC} = –4.5V to –5.5V		–11.0		µA/V
INPUT IMPEDANCE					
Resistance	Channel On		0.88		MΩ
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	f_B = 20kHz to 10MHz		4.0		nV/√Hz
Signal-to-Noise Ratio	S/N = 0.7/V_N • √5MHz		98		dB
INPUT VOLTAGE RANGE	Gain Error ≤ 10%		±4.2		V
TRANSFER CHARACTERISTICS	Voltage Gain				
	R_L = 1kΩ, V_{IN} = ±2V		0.982		V/V
	R_L = 10kΩ, V_{IN} = ±2.8V	0.98	0.992		V/V
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2.0		V_{CC}	V
Logic 0 Voltage		0		+0.8	V
Logic 1 Current	V_{SEL} = 5.0V		100	150	µA
Logic 0 Current	V_{SEL} = 0.8V		0.002	5	µA
SWITCHING CHARACTERISTICS	V_I = –0.3V to +0.7V, f = 5MHz				
SEL to Channel ON Time	90% Point of V_O = 1Vp-p		0.25		µs
SEL to Channel OFF Time	10% Point of V_O = 1Vp-p		0.25		µs
Switching Transient, Positive	Measured While Switching		+2.5		mV
Switching Transient, Negative	Between Two Grounded Channels		–1.2		mV
OUTPUT					
Voltage	V_{IN} = ±3V, R_L = 5kΩ	±2.8	±2.98		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		MΩ
Capacitance	No Channel Selected		1.5		pF
POWER SUPPLY					
Rated Voltage			±5		V
Derated Performance		±4.5		±5.5	V
Quiescent Current	One Channel Selected		±4.6	±5	mA
	No Channel Selected		±230	±350	µA
TEMPERATURE RANGE					
Operating, AP, AU		–40		+85	°C
Storage, AP, AU		–40		+125	°C
Thermal Resistance, θ_{JA}					
AP, AU			90		°C/W

SPECIFICATIONS

At V_{CC} = ±5V, R_L = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MPC100AP, AU MIN	MPC100AP, AU TYP	MPC100AP, AU MAX	UNITS
AC CHARACTERISTICS					
FREQUENCY DOMAIN					
LARGE SIGNAL BANDWIDTH (–3dB)	V_O = 5.0Vp-p, C_{OUT} = 1pF		70		MHz
	V_O = 2.8Vp-p, C_{OUT} = 1pF		140		MHz
	V_O = 1.4Vp-p, C_{OUT} = 1pF		250		MHz
SMALL SIGNAL BANDWIDTH	V_O = 0.2Vp-p, C_{OUT} = 1pF		450		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.05		%
	VDC = 0 to 1.4V		0.06		%
DIFFERENTIAL PHASE	f = 4.43MHz, V_{IN} = 0.3Vp-p				
	VDC = 0 to 0.7V		0.01		Degrees
	VDC = 0 to 1.4V		0.02		Degrees
GAIN FLATNESS PEAKING	V_O = 0.2Vp-p, DC to 30MHz		0.04		dB
	V_O = 0.2Vp-p, DC to 100MHz		0.05		dB
HARMONIC DISTORTION	f = 30MHz, V_O = 1.4Vp-p, R_L = 1kΩ				
Second Harmonic			–53		dBc
Third Harmonic			–67		dBc
CROSSTALK	V_I = 1.4Vp-p, Figures 4 and 8				
MPC100AP All Hostile	f = 5MHz,		–82		dB
	f = 30MHz,		–60		dB
Off Isolation	f = 5MHz,		–70		dB
	f = 30MHz,		–71		dB
MPC100AU All Hostile	f = 5MHz,		–78		dB
	f = 30MHz,		–70		dB
Off Isolation	f = 5MHz,		–75		dB
	f = 30MHz		–76		dB
TIME DOMAIN					
RISE TIME	V_O = 1.4Vp-p, Step 10% to 90%				
	C_{OUT} = 1pF, R_{OUT} = 22Ω		3.3		ns
SLEW RATE	V_O = 2Vp-p				
	C_{OUT} = 1pF		650		V/µs
	C_{OUT} = 22pF		460		V/µs
	C_{OUT} = 47pF		320		V/µs

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	±6V
Analog Input Voltage (IN_1 through IN_4)(1)	$\pm V_{CC}$, ±0.7V
Logic Input Voltage	–0.6V to $+V_{CC}$ +0.6V
Operating Temperature	–40°C to +85°C
Storage Temperature	–40°C to +125°C
Output Current	±6mA
Junction Temperature	+175°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL_1 through SEL_4)(1)	–0.5V to $+V_{CC}$ +0.7V

NOTE: (1) Inputs are internally diode-clamped to $\pm V_{CC}$.

PACKAGE/ORDERING INFORMATION

PRODUCT	TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER(1)
MPC100AP	–40°C to +85°C	14-Pin Plastic DIP	010
MPC100AU	–40°C to +85°C	SO-14 Surface Mount	235

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

FUNCTIONAL DESCRIPTION

IN_1-IN_4	Four analog input channels
GND	Analog input shielding grounds, connect to system ground
SEL_1 - SEL_4	Channel selection inputs
V_{OUT}	Analog output; tracks selected channel
$-V_{CC}$	Negative supply voltage; typical –5VDC
$+V_{CC}$	Positive supply voltage; typical +5VDC

ELECTROSTATIC DISCHARGE SENSITIVITY

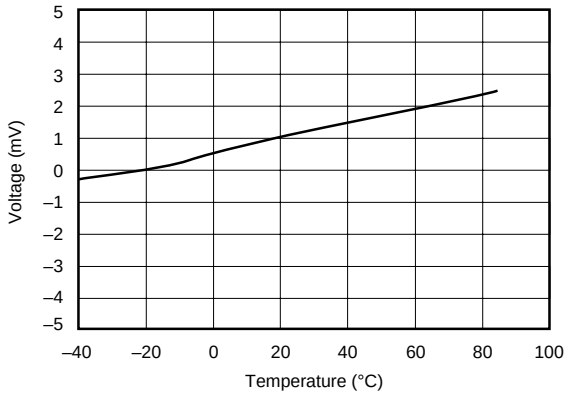
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

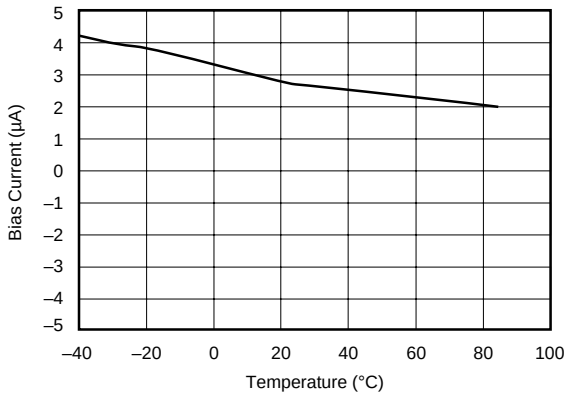
TYPICAL PERFORMANCE CURVES

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

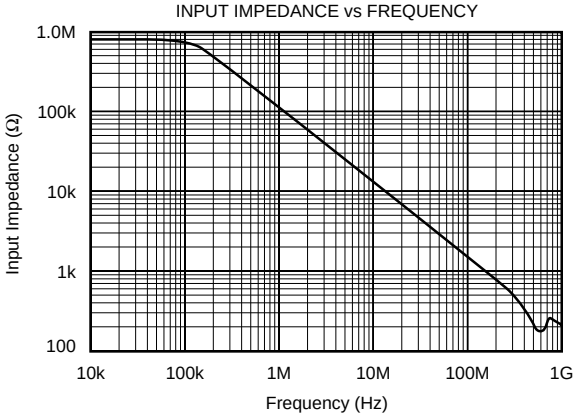
OFFSET VOLTAGE vs TEMPERATURE



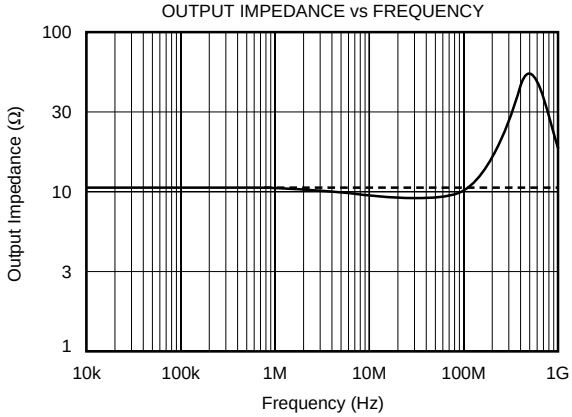
INPUT BIAS CURRENT vs TEMPERATURE



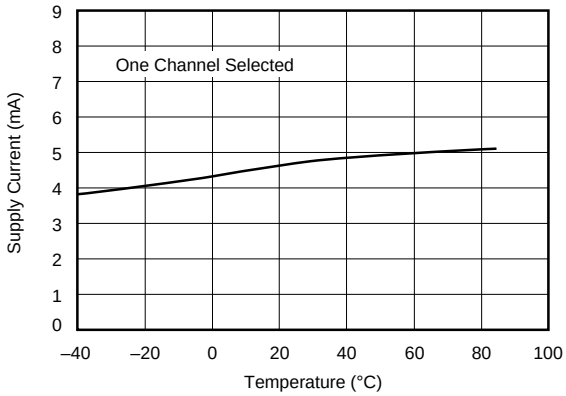
INPUT IMPEDANCE vs FREQUENCY



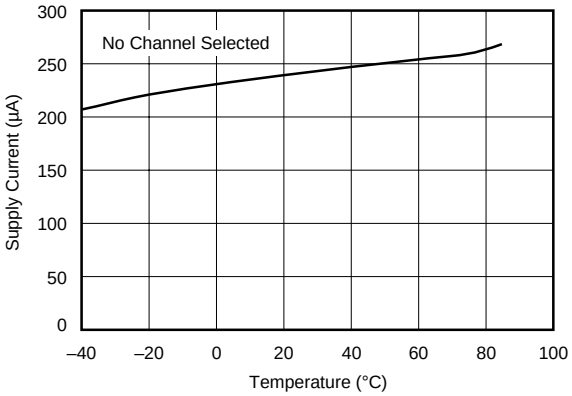
OUTPUT IMPEDANCE vs FREQUENCY



TOTAL QUIESCENT CURRENT vs TEMPERATURE



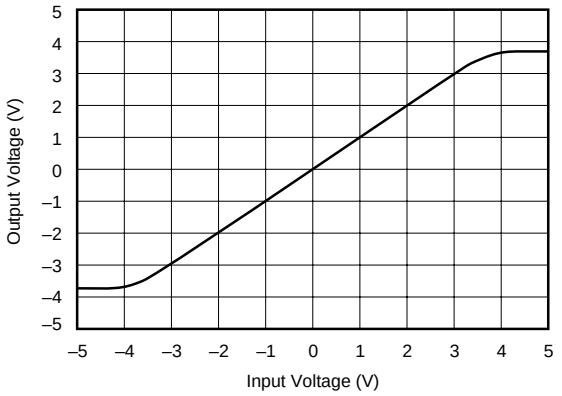
TOTAL QUIESCENT CURRENT vs TEMPERATURE



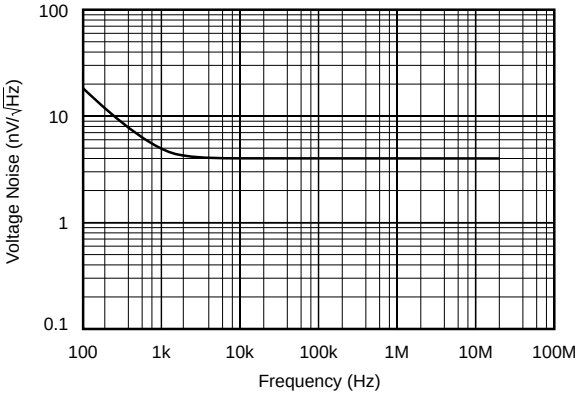
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

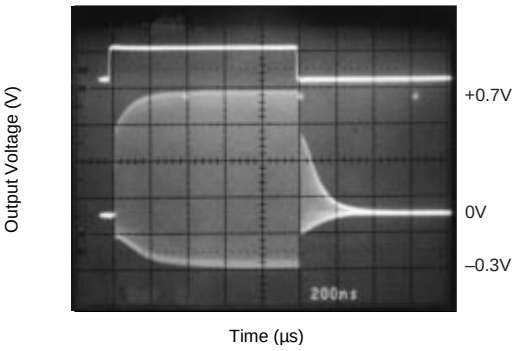
TRANSFER FUNCTION



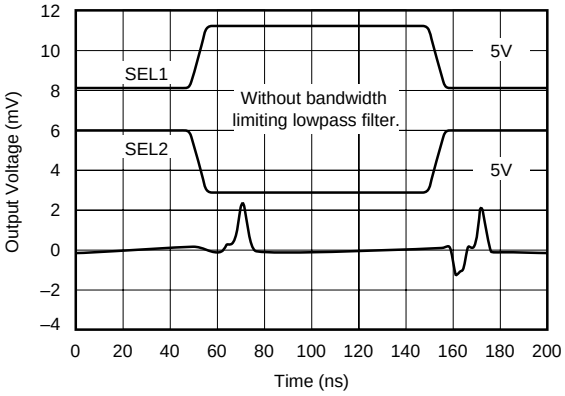
INPUT VOLTAGE NOISE SPECTRAL DENSITY



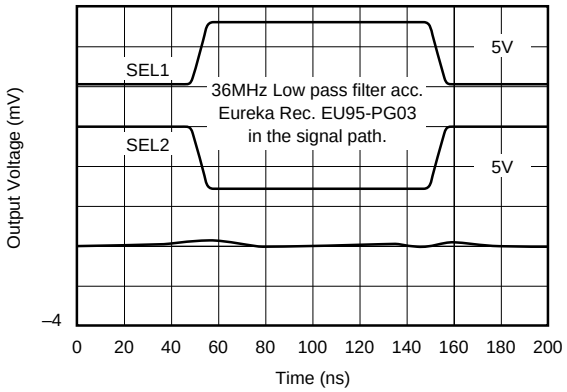
SWITCHING ENVELOPE (Video Signal)



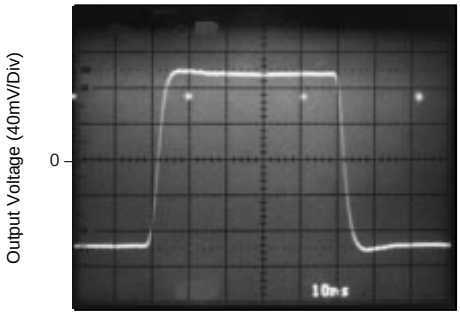
SWITCHING TRANSIENTS (Channel To Channel)



SWITCHING TRANSIENTS (Channel To Channel)



SMALL SIGNAL PULSE RESPONSE

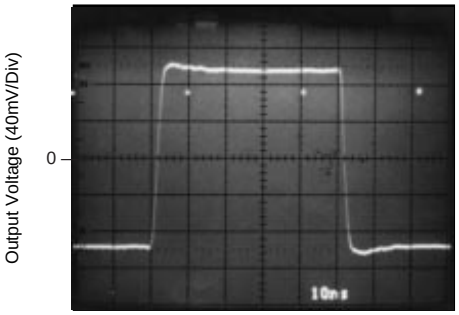


C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5VDC, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

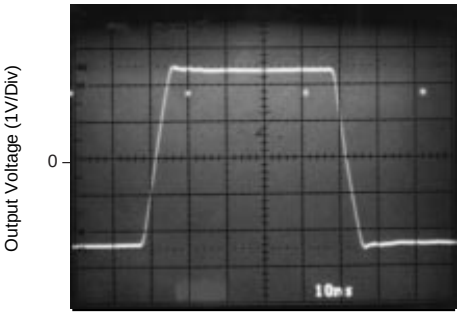
SMALL SIGNAL PULSE RESPONSE



Time (ns)

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 2ns
(Generator) V_I = 0.2Vp-p

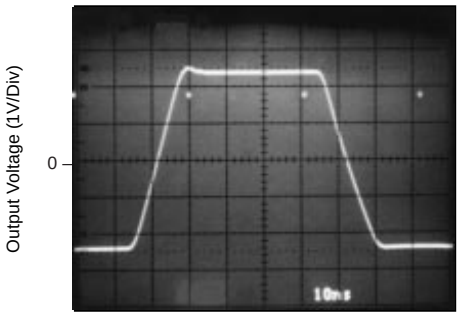
LARGE SIGNAL PULSE RESPONSE



Time (ns)

C_{OUT} = 1pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

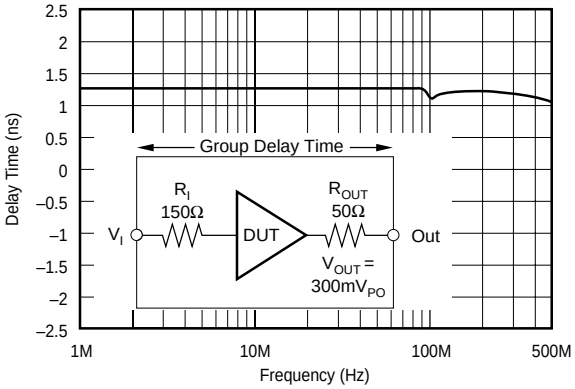
LARGE SIGNAL PULSE RESPONSE



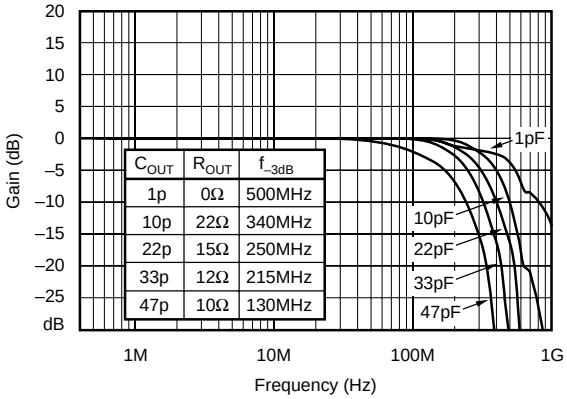
Time (ns)

C_{OUT} = 47pF, t_{RISE} = t_{FALL} = 5ns
(Generator) V_I = 5Vp-p

GROUP DELAY TIME vs FREQUENCY

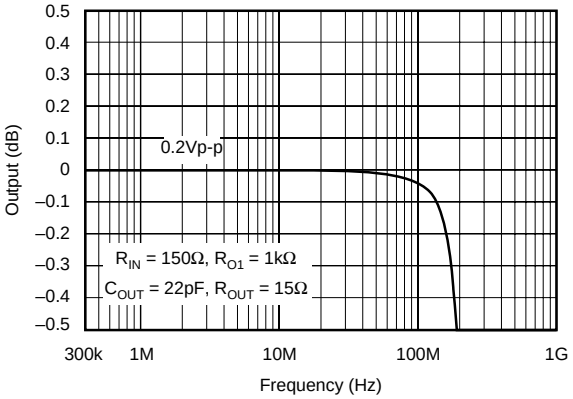


BANDWIDTH vs C_{OUT} WITH RECOMMENDED R_{OUT}



C_{OUT}	R_{OUT}	f_{-3dB}
1p	0Ω	500MHz
10p	22Ω	340MHz
22p	15Ω	250MHz
33p	12Ω	215MHz
47p	10Ω	130MHz

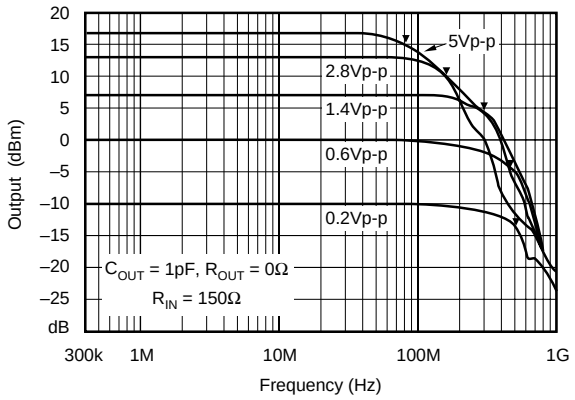
GAIN FLATNESS



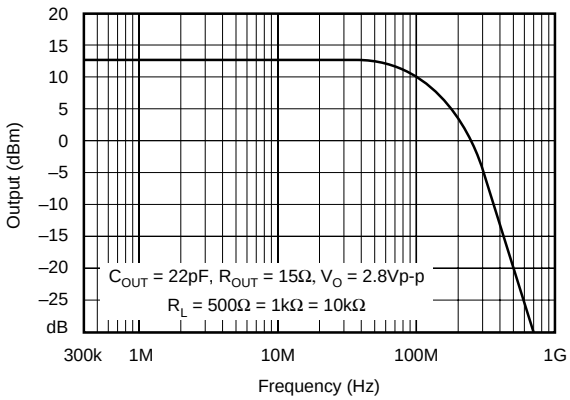
TYPICAL PERFORMANCE CURVES (CONT)

At V_{CC} = ±5V, R_{LOAD} = 10kΩ, R_{SOURCE} = 50Ω, and T_A = +25°C, unless otherwise noted.

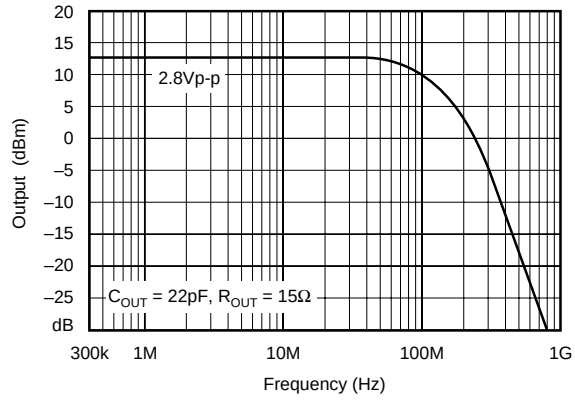
BANDWIDTH vs OUTPUT VOLTAGE



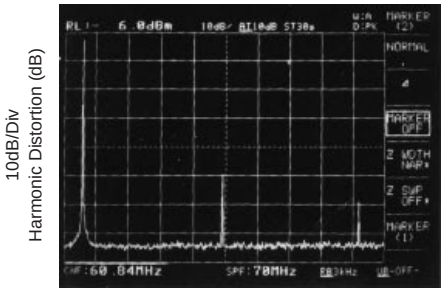
BANDWIDTH vs R_{LOAD}



BANDWIDTH MATCHING (DB1...DB4)



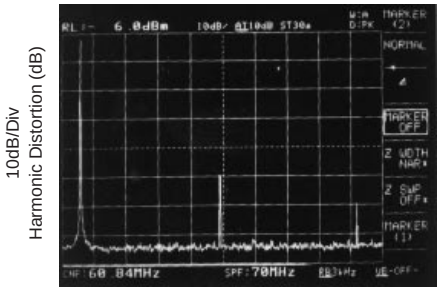
30MHz HARMONIC DISTORTION



Frequency (Hz)

V_{OUT} = 2.8Vp-p, R_L = 1kΩ, C_{OUT} = 1pF

30MHz HARMONIC DISTORTION



Frequency (Hz)

V_{OUT} = 2.8Vp-p, R_L = 10kΩ, C_{OUT} = 1pF

APPLICATIONS INFORMATION

The MPC100 operates from ±5V power supplies (±6V maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

All pins on the MPC100 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply as shown in Figure 1. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA or less whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision buffer amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC100.

Static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC100 incorporates on-chip ESD protection diodes as shown in Figure 1. This eliminates the need for the user to add external protection diodes, performance.

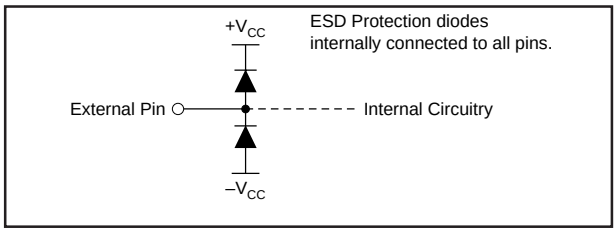


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC100 video multiplexer allows the user to connect any one of four analog input channels (IN_1-IN_4) to the output of the component and to switch between channels within less than 0.5µs. It consists of four identical unity-gain buffer amplifiers, which are connected together internally at the output. The open loop buffers consisting of complementary emitter followers applies no feedback, so their low frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form an unidirectional transmission path and thus provide high output-to-input isolation. Switching stages compatible to TTL level digital signals are provided for each buffer to select the input channel. When no channel is selected, the output of the device is high-impedance and allows the user to wire more MPC100s together to form switch multi-channel matrices.

If one channel is selected with a digital "1" at the corresponding SEL-input, the MPC100 acts as a buffer amplifier with high input impedance and low output impedance. The truth table on the front page describes the relationship between the digital inputs (SEL_1 to SEL_4) and the analog inputs (IN_1 to IN_4), and which signal is selected at the output.

The 2-4 address decoder and chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases BUS-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. It requires DC coupling and termination resistors when directly driven from a low impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. The single chip bandwidth of over 250MHz at an output voltage of 1.4Vp-p allows the design of large crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.05%) and phase (0.01°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the brightness (luminance) signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity, and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC100 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it interferes only minimally with the input signals.

The transient peaks remain less than +2.5mV and –1.2mV. Subsequent equipment might interpret large negative output glitches as synchronization pulses. To remove this problem, the output must be clamped during the switching dead time. With the MPC100, the generated output transients are extremely small and clamping is unnecessary. The switching time between two channels is less than 0.5µs. This short time period allows easy switching during the vertical blanking time. The signal envelope during the transition from one channel to another rises and falls symmetrically and shows less overshooting or DC settling transients.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Most of the buffers are always in off-state. One important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of ±230µA in off-state and ±4.6mA when one channel is selected, as well as the reduced ±5V supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC100 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately 2.2µF), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance or inductance.
- Make short and low inductance traces. The entire physical circuit layout should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection. Refer to the suggested layout shown in Figure 6.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended because they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile solderless sockets.
- Use low-inductance and surface-mounted components to achieve the best AC-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential.

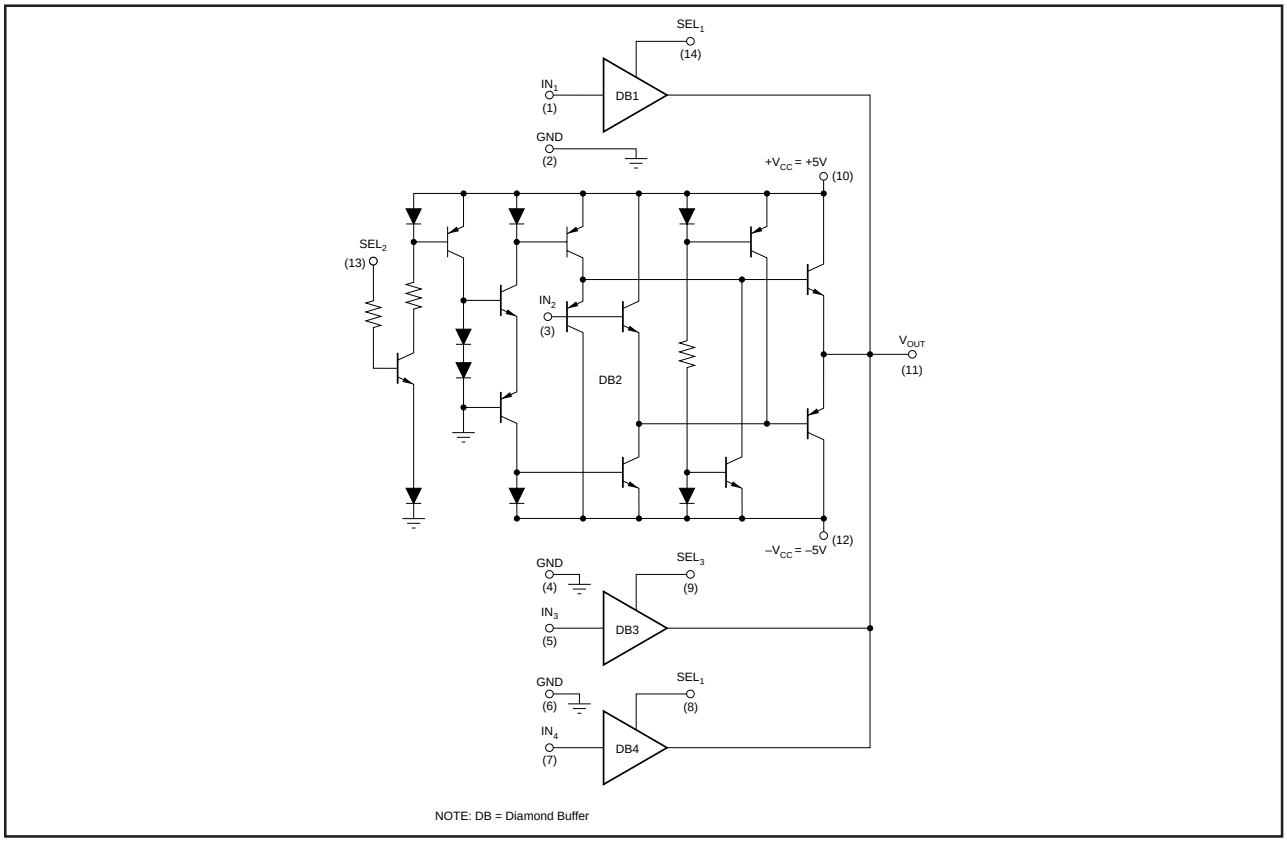


FIGURE 2. Simplified Circuit Diagram.

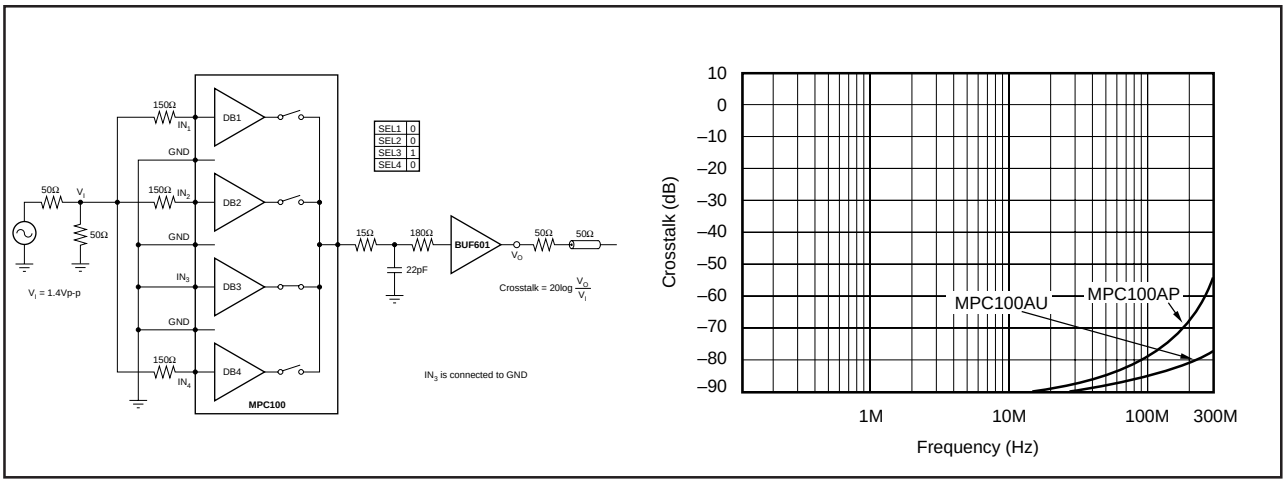


FIGURE 3. Channel Crosstalk—Grounded Input.

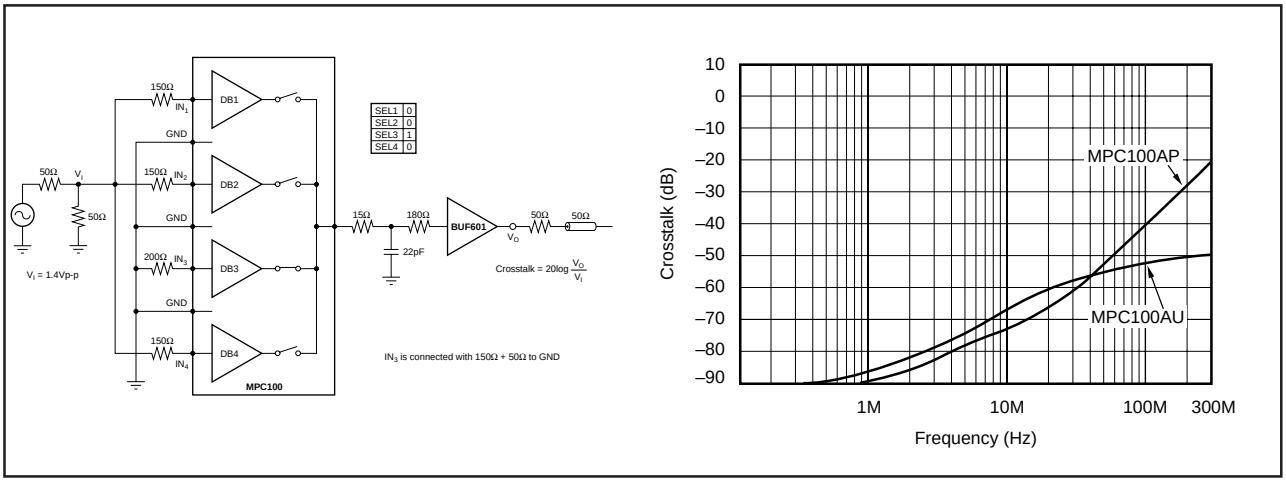


FIGURE 4. Channel Crosstalk—150Ω Input Resistor.

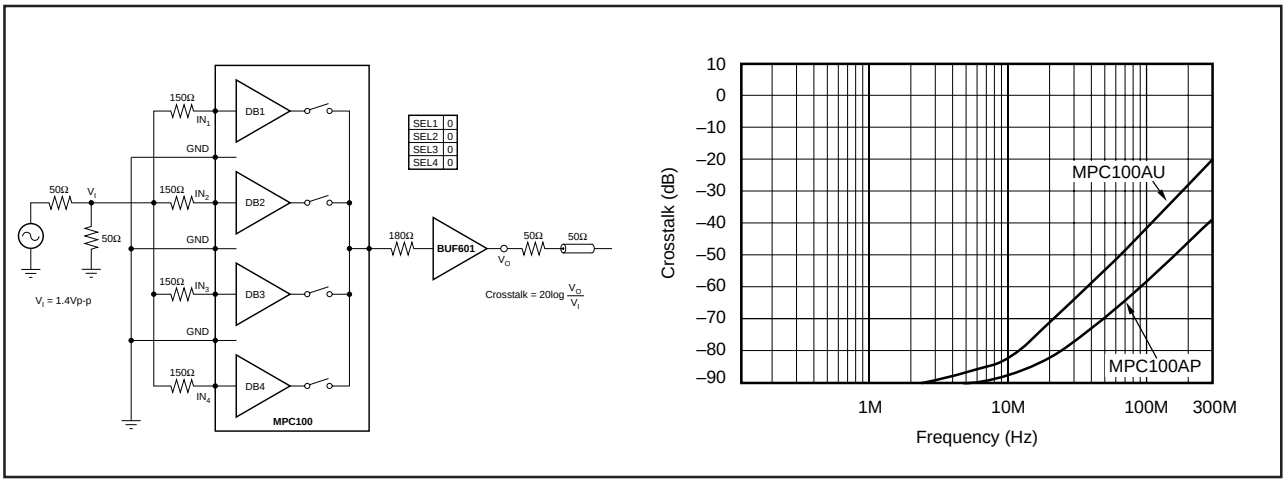


FIGURE 5. Off Isolation.

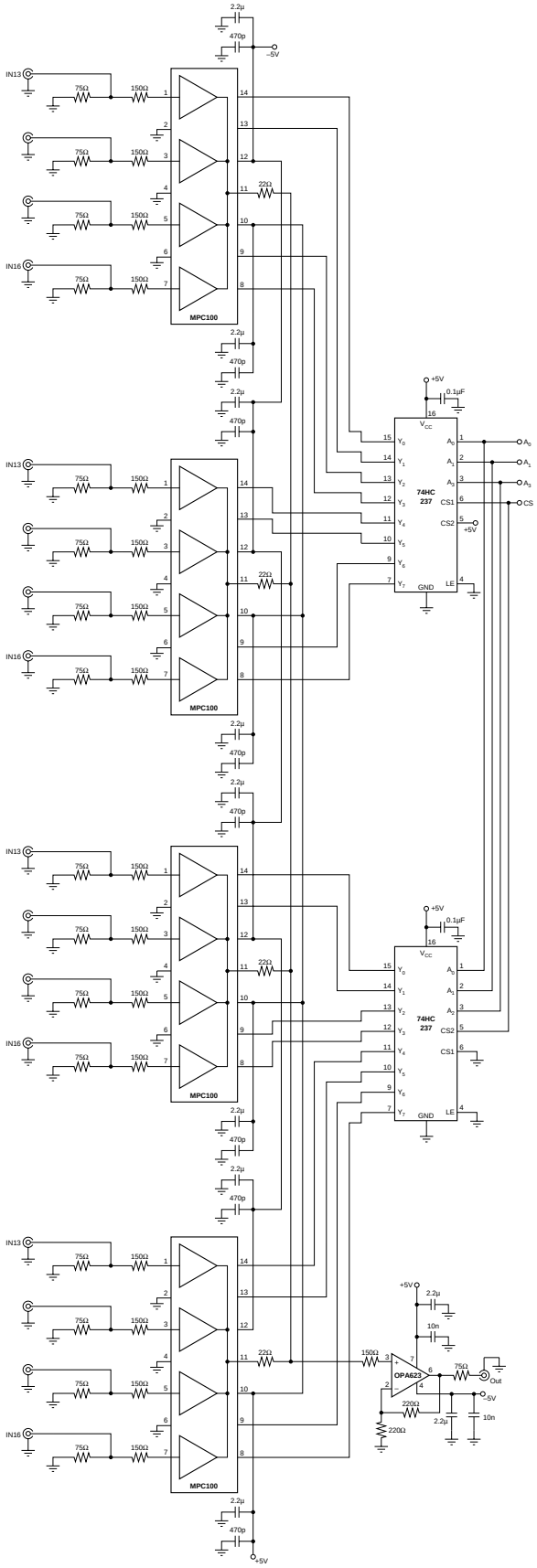
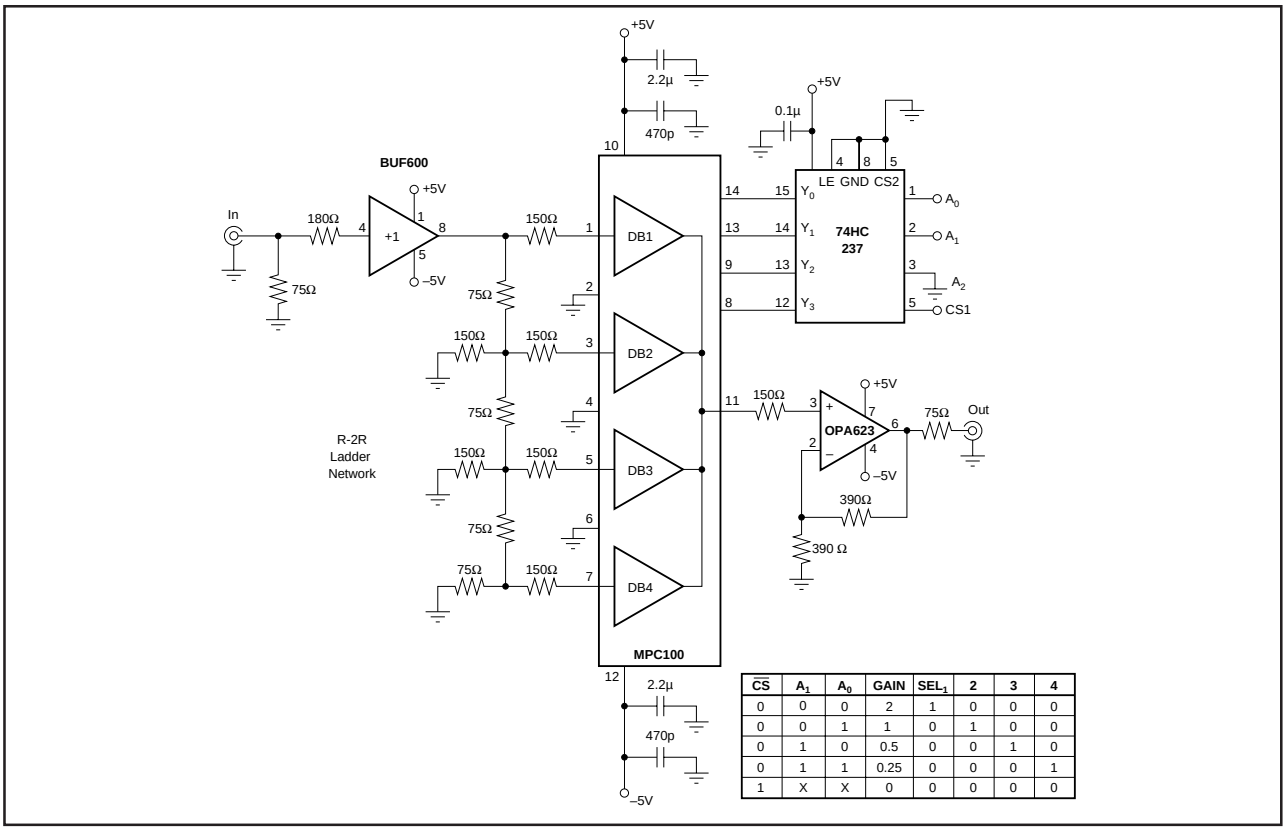


FIGURE 6. Video Distribution Field.



$\overline{CS}$	A_1	A_0	GAIN	SEL_1	2	3	4
0	0	0	2	1	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0.5	0	0	1	0
0	1	1	0.25	0	0	0	1
1	X	X	0	0	0	0	0

FIGURE 7. Digital Gain Control.

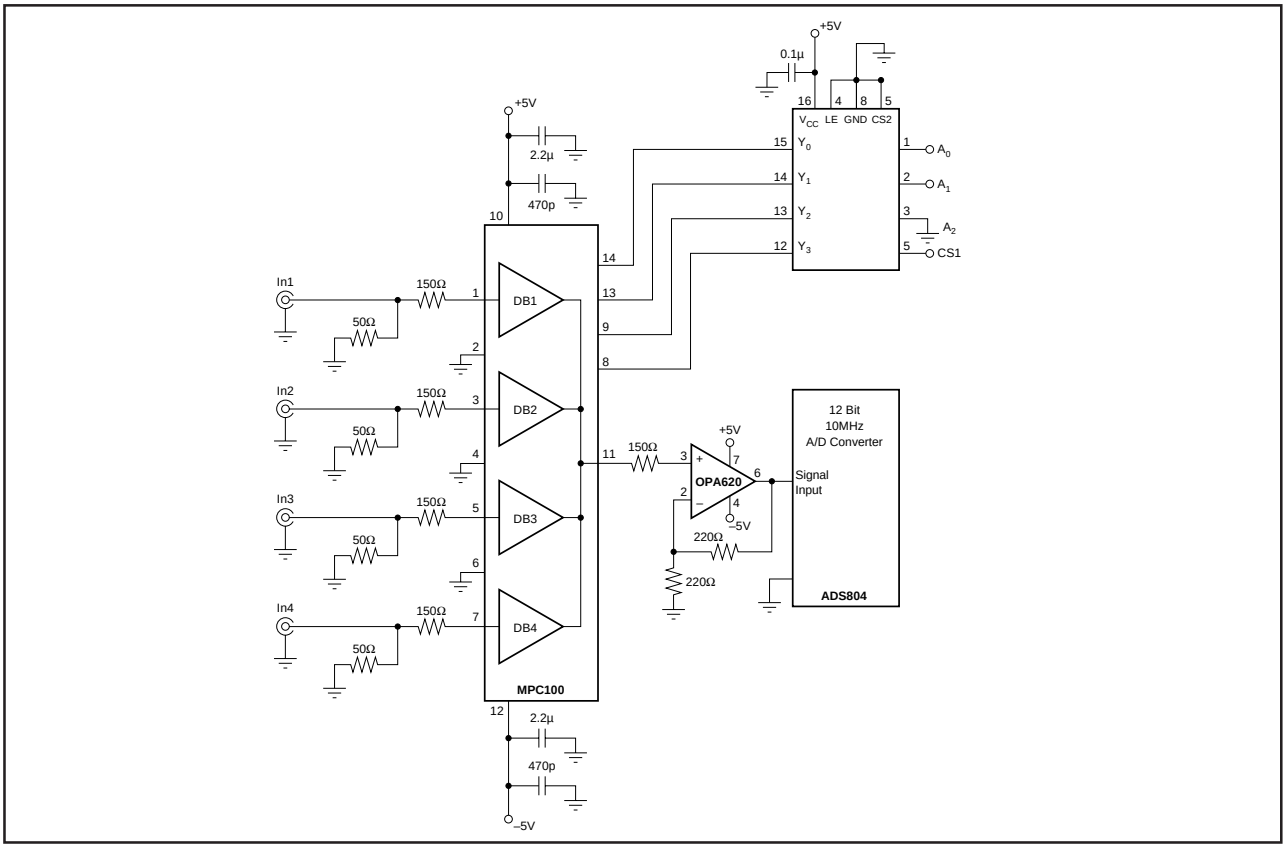


FIGURE 8. High Speed Data Acquisition System.

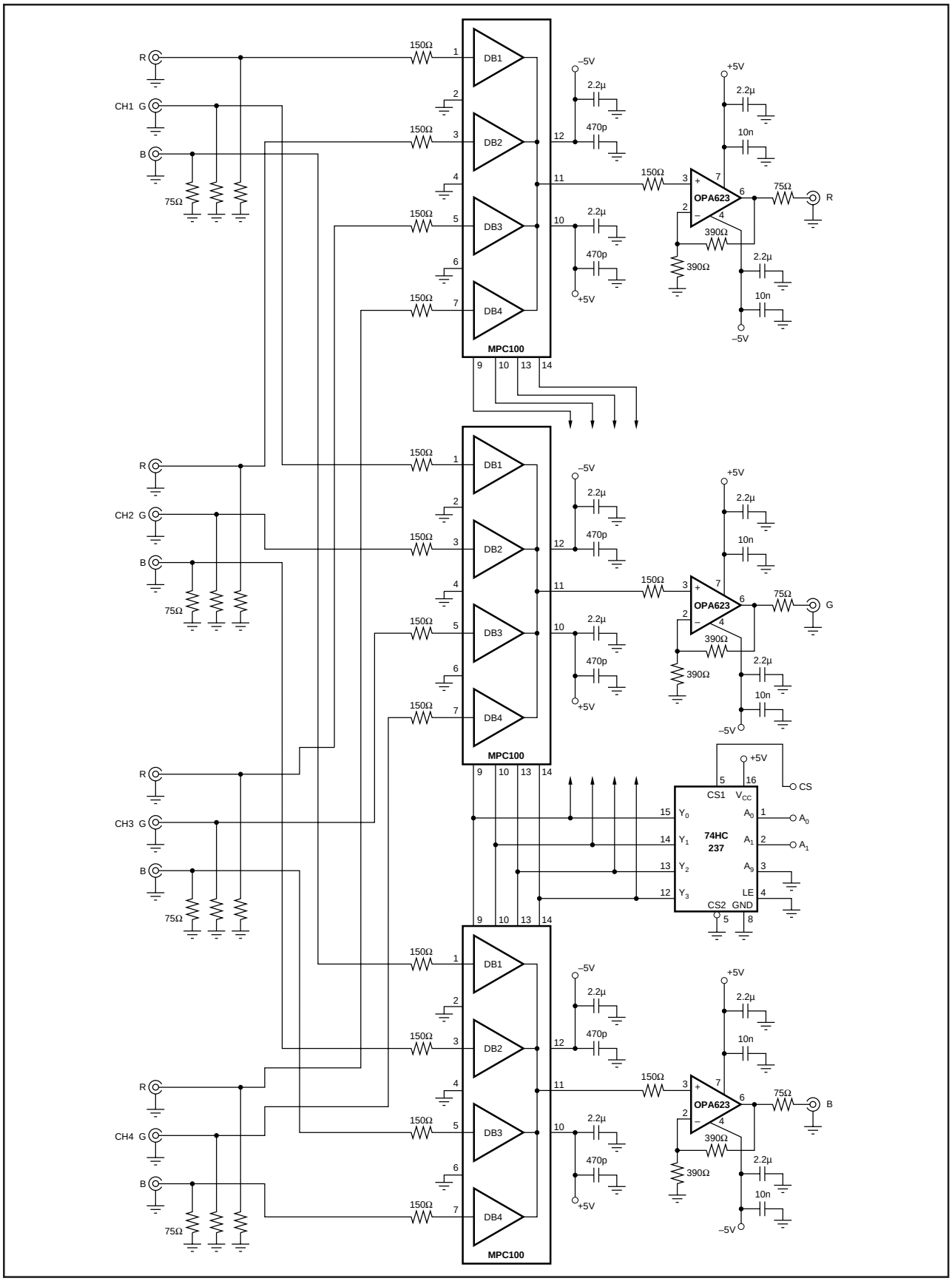


FIGURE 9. Distribution Field for High Resolution Graphic Cards, Cameras.

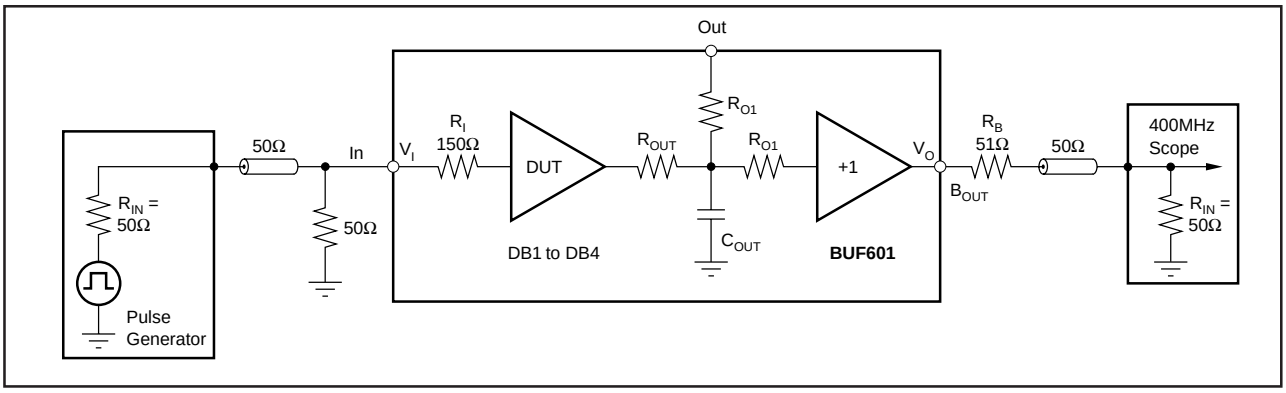


FIGURE 10. Test Circuit Pulse Response.

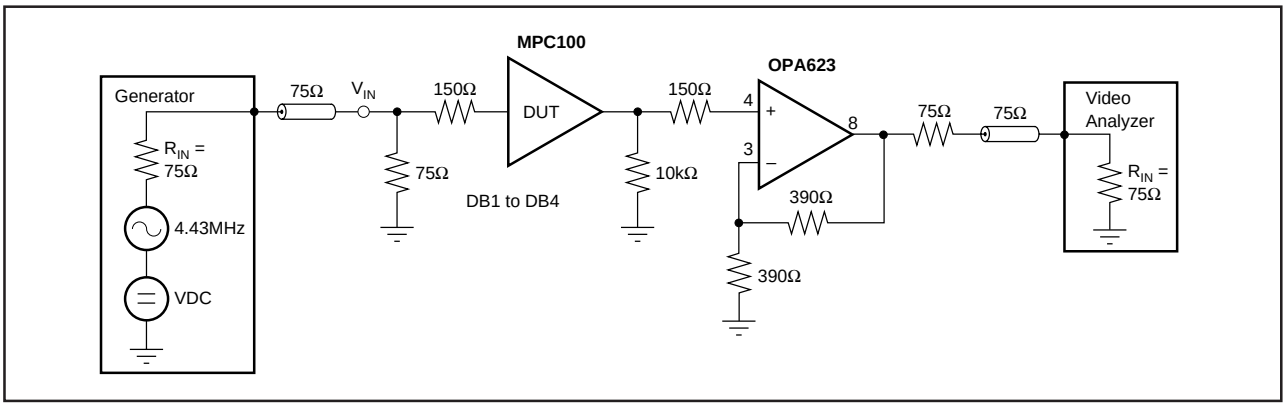


FIGURE 11. Test Circuit Differential Gain and Phase.

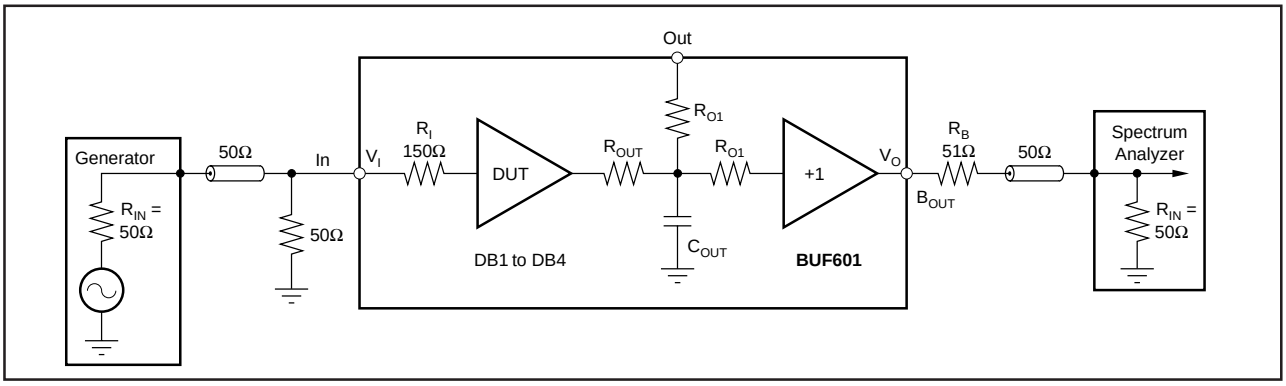


FIGURE 12. Test Circuit Frequency Response.

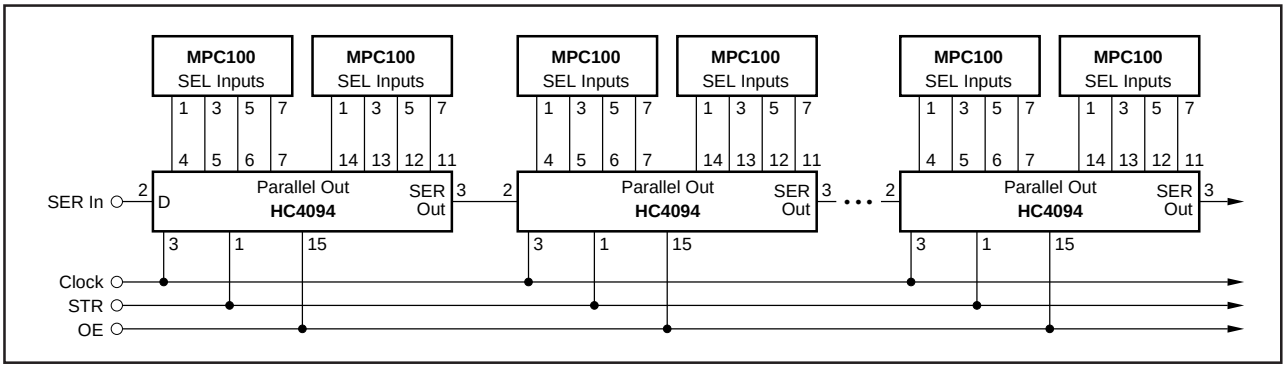


FIGURE 13. Serial Bus-Controlled Distribution Field.

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